

SOLVING CONSTRAINT SATISFIABILITY PROBLEM FOR AUTOMATIC GENERATION OF DESIGN VERIFICATION VECTORS

Chung-Yang Huang

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ABSTRACT

A method for generating a test vector for functional verification of circuits includes providing a representation of a circuit, where the representation includes a control logic component and a datapath logic component. The method also includes reading one or more vector generation targets, and performing word-level ATPG justification on the control logic component to obtain a control logic solution. The method further includes extracting one or more arithmetic functions for the datapath logic component based on the control logic solution, and solving the one or more arithmetic functions using a modular constraint solver. The modular constraint solver is based on a modular number system.

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